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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,850	09/04/2003	Wun Wang	JCLA11354	7076

7590 11/01/2004

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EXAMINER	
FRANK, ELLIOT L	
ART UNIT	**PAPER NUMBER**
2125	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,850	WANG, WUN	
	Examiner	Art Unit	
	Elliot L Frank	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Ex Parte Quayle Action

1. This application is in condition for allowance except for the following formal matters:

    a. The disclosure is objected to because of the following informalities:

        i. Page 3, line 16: The phrase "in control table" should be corrected to "in a control table".

        ii. Appropriate correction is required.

    b. The errors noted by the examiner may not constitute all of the aberrations in the specification. The applicant is encouraged to thoroughly review the specification and correct any informality encountered.

    c. Claims 1-10 are objected to because of the following informalities:

        i. Claim 1, line 7: There is a minor grammatical issue. Please insert the word "of" after the word "each ".

        ii. Claim 1, line 8: There is a minor grammatical issue. Please insert the word "as" after the word "indicated ".

        iii. Claim 1, lines 16-17: The term "defect impact contribution" should be corrected to "yield impact contribution" to maintain the uniformity of the claim language.

        iv. Claims 2-10 depend from claim 1 and are also objected to for containing the same deficiencies.

    Appropriate correction is required.

Allowable Subject Matter

2. Claims 1-10 contain allowable subject matter.

   a. The prior art, taken singly or in any reasonable combination, fails to teach or fairly suggest the claimed invention.

   b. Claims 1-10 are currently pending in the application and depend from claim 1. Claim 1 has the following requirements:

      A method for determining yield loss of process steps for semiconductor wafers having a plurality of dies, the method comprising:

      inspecting the dies of the semiconductor wafers to determine a defect type and a defect count for each the defect type;

      electrical testing the dies of the semiconductor wafers to determine a fail die and a pass die, wherein each the fail die having a single defect or a plurality of defects is indicated a hit;

      determining a defect calibrated factor for eliminating defect count excursions in a yield control table for the semiconductor wafers, wherein the defect calibrated factor is based on a difference between a ratio of the hits to a quantity of the dies with defects and a ratio of a quantity of the fail dies without defects to a quantity of the pass dies without defects;

      weighting a hit ratio with a function of the defect counts of the defect type, wherein the hit ratio is ratio of the hits of the defect type to the defect counts of the defect type;

determining a yield impact contribution for each of the defect types, wherein the defect impact contribution is based on a calibrated ratio of the weighted hit ratio for each of the defect types to a sum of the weighted hit ratio for all of the defect types;

determining a kill ratio for each of the defect types, wherein the kill ratio is based on a yield impact calibrated factor for the defect types, a total quantity of the defect counts, an average defect density of the defect types, and a die area; and

determining a yield loss for each of the defect types, wherein the yield loss is based on the kill ratio for the defect type, the average defect density of the defect type, the die area, and the yield impact calibrated factor.

c. The most relevant prior art of record is US 6,496,958 B1 to Ott et al., which incorporates by reference US 6,367,040 B1 also to Ott et al. The '040 patent includes the earlier steps required by claim 1 including classifying and counting defects, correlating these results to electrical test failures in order to determine hits, and determining a weighted hit ratio (column 2, lines 30-35 and column 6, line 8-20, wherein the calculation of the "kill ratio" of Ott et al. is deemed to be analogous to the "weighted hit ratio" of the instant invention given the similarity between the terms). The ' 958 incorporates the steps of the '040 patent and further calculates a yield loss (depicted in figure 1).

d. The combined '040 and '958 patents are deficient because neither discuss the calculation of defect calibrated factor as required by claim 1:

"determining a defect calibrated factor for eliminating defect count excursions in a yield control table for the semiconductor wafers, wherein the defect calibrated factor is based on a difference between a ratio of the hits to a quantity of the dies with defects and a ratio of a quantity of the fail dies without defects to a quantity of the pass dies without defects."

This factor is carried throughout the calculation of yield loss in claim 1 in order to deliver a more precise yield loss than the prior art methods (Specification, page 3, paragraph 9).

e. Additional searches of both patent and non-patent literature focusing on the defect calibrated factor requirement of claim 1 did not reveal any references that anticipate or make obvious this requirement.

f. Therefore, the limitations of claim 1, in combination with the remaining elements and features of the instant invention, were not disclosed nor fairly suggested by the prior art of record.

Conclusion

3. Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US 2002/0002415 A1 – Mugibayashi et al. – Defect analysis

USPN 6,367,040 B1 – Ott et al. – Defect analysis

USPN 6,496,958 B1 – Ott et al. – Defect analysis

USPN 6,613,590 B2 – Simmons – Defect analysis

USPN 6,717,431 B2 – Rathei et al. – Defect analysis

Patterson, O.D., Hansen, M.H., "The impact of tolerance on kill ratio estimation for memory", Advanced Semiconductor Manufacturing Conference and Workshop, 2000 IEEE/SEMI , 12-14 Sept. 2000, Pages:175 – 180.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elliot L Frank whose telephone number is (571) 272-3739. The examiner can normally be reached on M-F 8-5:00 (flex).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (571) 373-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ELF
31 October 2004

ELLIOT FRANK
PATENT EXAMINER 10/31/04